AMENDMENTS TO THE CLAIMS

Please find below a complete listing of the claims in the application, including their status as effected by the present amendment:

1) – 14) (cancelled)

15) (currently amended) A switch fabric implemented on a chip, comprising: [[~~as defined in claim 14,~~]]

a) an array of cells;

b) an I/O interface in communication with said array of cells for permitting exchange of data packets between said array of cells and components external to said array of cells;

c) each cell including:

I) a transmitter in communication with said I/O interface and in communication with every other cell of said array, said transmitter operative to process a data packet received from said I/O interface to determine a destination of the data packet and forward the data packet to at least one cell of said array selected on a basis of the determined destination;

II) a plurality of receivers associated with respective cells from said array, each receiver being in communication with a respective cell allowing the respective cell to forward data packets to the receiver;

III) said receivers in communication with said I/O interface for releasing data packets to said I/O interface;

wherein said array of cells includes a plurality of data channels, each data channel being associated with a given cell, the data channel associated with said given cell connecting the transmitter of said given cell to receivers in cells other than said given cell and associated with said given cell;

wherein the transmitter of said given cell includes a memory for storing data packets received from said I/O interface;

wherein said memory includes a plurality of segments, each segment being associated with a receiver in a cell of said array to which the transmitter of said given cell is capable of forwarding a data packet via the data channel associated with said given cell;

wherein the transmitter of said given cell includes a control entity that processes a data packet forwarded from said I/O interface to determine a cell of said array to which the packet is destined and identify on a basis of the determined cell a segment of said memory into which the packet is to be loaded;

wherein said control entity includes a plurality of queue controllers associated with respective segments of said memory;

wherein said memory implements a plurality of registers, each register being associated with a queue controller and being suitable for holding data representative of a degree of occupancy of a segment of said memory associated with the queue controller;

wherein a data packet received by said transmitter from said I/O interface is characterized by a priority level selected from a group of priority levels, each segment of said memory being partitioned into slots, each slot being capable of storing at least one data packet, each slot being associated with a given priority level of said group of priority levels.

16) (original) A switch fabric as defined in claim 15, wherein the registers of said memory associated with each queue controller store data indicative of a degree of occupancy of the slots of said segment associated with the queue controller, for each priority level of the group of priority levels.

17) (currently amended) A switch fabric implemented on a chip, comprising: [[~~as defined in claim 12,~~]]

a) an array of cells;

b) an I/O interface in communication with said array of cells for permitting exchange of data packets between said array of cells and components external to said array of cells;

c) each cell including:

I) a transmitter in communication with said I/O interface and in communication with every other cell of said array, said transmitter operative to process a data packet received from said I/O interface to determine a destination of the data packet and forward the data packet to at least one cell of said array selected on a basis of the determined destination;

II) a plurality of receivers associated with respective cells from said array, each receiver being in communication with a respective cell allowing the respective cell to forward data packets to the receiver;

III) said receivers in communication with said I/O interface for releasing data packets to said I/O interface;

wherein said array of cells includes a plurality of data channels, each data channel being associated with a given cell, the data channel associated with said given cell connecting the transmitter of said given cell to receivers in cells other than said given cell and associated with said given cell;

wherein the transmitter of said given cell includes a memory for storing data packets received from said I/O interface;

wherein said memory includes a plurality of segments, each segment being associated with a receiver in a cell of said array to which the transmitter of said given cell is capable of forwarding a data packet via the data channel associated with said given cell;

wherein the transmitter of said given cell includes a control entity that processes a data packet forwarded from said I/O interface to determine a cell of said array to which the packet is destined and identify on a basis of the determined cell a segment of said memory into which the packet is to be loaded;

wherein the transmitter of said given cell communicates with each receiver associated with said given cell to assess a degree of occupancy of each receiver associated with said given cell.

18) (original) A switch fabric as defined in claim 17, wherein the transmitter of said given cell communicates with each receiver associated with said given

cell to assess the degree of occupancy of each receiver associated with said given cell over a back channel.

19) (original) A switch fabric as defined in claim 18, including a plurality of back channels, there being a dedicated back channel between the transmitter of said given cell and each receiver associated with said given cell.

20) (original) A switch fabric as defined in claim 19, wherein each back channel transfers data serially.

21) (original) A switch fabric as defined in claim 18, wherein said memory includes an area for storing data indicative of the degree of occupancy of each receiver associated with said given cell.

22) (original) A switch fabric as defined in claim 21, wherein said control entity is operative to process the data indicative of the degree of occupancy of each receiver associated with said given cell to determine which data packet stored in said memory is suitable for transmission to a receiver.

23) (original) A switch fabric as defined in claim 22, wherein said control entity determines that a data packet is suitable for transmission to a certain receiver when the data indicative of the degree of occupancy of the certain receiver indicates that the receiver is capable of accepting the data packet.

24) (original) A switch fabric as defined in claim 23, wherein when said control entity determines that a data packet is suitable for transmission, said control entity generates a control signal to request transmission of the data packet.

25) (original) A switch fabric as defined in claim 24, wherein when said control entity determines that a plurality of data packets are suitable for transmission, said control entity generates a plurality of control signals to request transmission of the data packets, each control signal being associated with a data packet.

26) (original) A switch fabric as defined in claim 25, wherein said control entity includes an arbiter for processing said control signals to select a data packet to transmit among the plurality of data packets suitable for transmission.

27) (original) A switch fabric as defined in claim 26, wherein a data packet is characterized by a priority level, wherein each control signal conveys the priority level of the data packet associated with the control signal.

28) (original) A switch fabric as defined in claim 27, wherein said arbiter selects a data packet to transmit among the plurality of data packets suitable for transmission on a basis of the priority levels of the plurality of data packets suitable for transmission.

29) (original) A switch fabric as defined in claim 28 wherein said arbiter processes control signals to request transmission of data packets in a round robin manner.

30) (original) A switch fabric as defined in claim 29, wherein said arbiter selects a data packet to transmit among the plurality of data packets suitable for transmission on a basis of the priority levels of the plurality of data packets suitable for transmission and on the basis of whether or not a data packet was previously submitted for transmission.

31) (currently amended) A switch fabric <u>implemented on a chip, comprising:</u> [[~~as defined in claim 10,~~]]

<u>a) an array of cells;</u>

<u>b) an I/O interface in communication with said array of cells for permitting exchange of data packets between said array of cells and components external to said array of cells;</u>

<u>c) each cell including:</u>

<u>I) a transmitter in communication with said I/O interface and in communication with every other cell of said array, said transmitter operative to process a data packet received from said I/O interface to determine a destination of the data</u>

packet and forward the data packet to at least one cell of said array selected on a basis of the determined destination;

II) a plurality of receivers associated with respective cells from said array, each receiver being in communication with a respective cell allowing the respective cell to forward data packets to the receiver;

III) said receivers in communication with said I/O interface for releasing data packets to said I/O interface;

wherein said array of cells includes a plurality of data channels, each data channel being associated with a given cell, the data channel associated with said given cell connecting the transmitter of said given cell to receivers in cells other than said given cell and associated with said given cell;

wherein the transmitter of said given cell includes a memory for storing data packets received from said I/O interface;

wherein said memory is a first memory, said cell comprising a second memory including a plurality of sectors associated with respective receivers of said plurality of receivers, said sectors being capable of storing data packets forwarded to said receivers by cells of said array.

32) (original) A switch fabric as defined in claim 31, wherein each receiver of said plurality of receivers communicates with said I/O interface.

33) (original) A switch fabric as defined in claim 31, wherein said plurality of receivers includes a control entity to regulate a release of data packets from said sectors to said I/O interface.

34) (original) A switch fabric as defined in claim 33, wherein said control entity includes a plurality of queue controllers associated with respective sectors of said memory.

35) (original) A switch fabric as defined in claim 34, wherein a data packet received by a receiver of said plurality of receivers is characterized by a priority level selected from a group of priority levels, each sector of said

second memory being divided into subdivisions, each subdivision being capable of storing at least one data packet, each subdivision being associated with a given priority level of said group of priority levels.

36) (original) A switch fabric as defined in claim 35, wherein said control entity includes an arbiter in communication with said queue controllers, each queue controller being operative to transmit a control signal to said arbiter for each data packet held in the sector associated with the queue controller to request release of the data packet to said I/O interface.

37) (original) A switch fabric as defined in claim 36, wherein each control signal conveys the priority level of the data packet associated with the control signal.

38) (original) A switch fabric as defined in claim 37, wherein said arbiter selects a data packet for release to said I/O interface among the data packets corresponding to the control signals transmitted to said arbiter on the basis of the levels of priority of the data packets corresponding to the control signals transmitted to said arbiter.

39) (currently amended) A switch fabric implemented on a chip, comprising: [[~~as defined in claim 1,~~]]

a) an array of cells;

b) an I/O interface in communication with said array of cells for permitting exchange of data packets between said array of cells and components external to said array of cells;

c) each cell including:

I) a transmitter in communication with said I/O interface and in communication with every other cell of said array, said transmitter operative to process a data packet received from said I/O interface to determine a destination of the data packet and forward the data packet to at least one cell of said array selected on a basis of the determined destination;

II) a plurality of receivers associated with respective cells from said array, each receiver being in communication with a respective cell allowing the respective cell to forward data packets to the receiver;

III) said receivers in communication with said I/O interface for releasing data packets to said I/O interface;

wherein each data packet comprises a plurality of words including a first word of said data packet and a last word of said data packet, wherein each word comprises a field indicative of whether said word is a pre-determined number of words away from said last word of said data packet.

40) (original) A switch fabric as defined in claim 39, wherein the transmitter is operative to monitor said field in each word of each data packet forwarded to at least one cell of said array, the transmitter further being operative to begin forwarding a next data packet upon detecting that said field of a word in a packet currently being forwarded is indicative of said word being a pre-determined number of words away from the last word of said data packet currently being forwarded.

41) - 44) (cancelled)

45) (original) A switch fabric as defined in claim 25, each cell further including a central processing unit (CPU) connected to the plurality of receivers, wherein said control entity includes a first arbiter for processing said control signals to select a data packet to transmit to the I/O interface among the plurality of data packets suitable for transmission to the I/O interface, wherein said control entity includes a second arbiter for processing said control signals to select a data packet to transmit to the CPU among the plurality of data packets suitable for transmission to the CPU.

46)(cancelled)

47)(cancelled)